Frequency Divider Design for a GPSDO

Introduction

A GPS Disciplined Oscillator typically produces a 10MHz output. It is often useful to have additional frequencies that are a sub-multiple of the 10MHz signal available.

I wanted a frequency divider that would provide low jitter or phase noise when fed with the output of a Trimble Thunderbolt GPS disciplined oscillator. The 10MHz output of the Thunderbolt is a sinusoidal signal at a level of +12.5dBm +/- 2.5dBm into 50 ohms. This is about 2.5V peak to peak.

I decided that I wanted to provide square ware output signals at 10MHz, 5MHz, 1MHz, and one output with the output frequency selectable from 100kHz to 1Hz in decades. The output level should be 5V into 1MΩ and 2.5V into 50Ω.

I am indebted to Bruce Griffiths and others on the "time-nuts" mailing list for assistance with and constructive criticism of the design. All faults are my own (with a little help from the schematic capture and layout software).

Design for the input clock shaper.

The main divider circuit requires a 10MHz square wave input clock signal at CMOS signal levels. The Trimble Thunderbolt output is a sine wave at about 2.5V peak to peak. So it is necessary to use a clock shaper circuit to convert the input sine wave to a square wave clock signal. The design used is a capacitively coupled input driving an ADCMP600 or MAX999 comparator (either may be used). The design is from Bruce Griffiths' web page on clock shapers:

http://www.ko4bb.com/~bruce/CLKSHPR.html

The circuit has a wide bandwidth [<10kHz, > 100MHz], and the input amplitude range is [100mV - 5V]p-p.

The clock shaper circuit was originally designed for use in a linear phase detector there are other applications for which it is suitable. It is derived from the input clock shaping circuit in the HP K34-5991A. An ADCMP600 (or MAX999) comparator with a CMOS/TTL compatible output is substituted for the ECL differential amplifiers in the K34-5991A.

Design for the frequency divider.

The frequency divider is based around the use of a 74AC163 counter configured to divide by ten to derive the 5MHz and 1MHz output signals. The 74AC163 was chosen in preference to the 74HC163 as the chip delays are lower in the 74AC163. The lower frequency signals are derived from the 1MHz output of the 74AC163 using a chain of 74HC4017s.

The 5MHz output is taken directly from the QA output of the 74AC163 and re-clocked to the 10MHz clock signal using a 74AC74 D-type flip-flop. The signal is re-clocked again in the second half of the 74AC74 to delay the signal by one additional 10MHz clock cycle.

The 1MHz signal is derived from the "Ripple Count Out" (RCO) output of the 74AC163. This signal is a pulse signal, not a square wave. This is converted to a square wave using a 74AC164 shift register (serial in parallel out) and a 74AC112 J-K flip-flop. The signal is then re-clocked again in the other half of the 74AC112 to delay the signal by one additional 10MHz clock cycle.

The double clocking of the 5MHz and 1MHz outputs is so that the rising edges will be aligned with the rising edges of the low frequency outputs, the derivation of which is described below.

The 1MHz output is further divided down by a chain of six 74HC4017 Johnson Counters connected as a ripple divider which provides outputs from 100kHz down to 1Hz. A 74HC4051 analogue multiplexor is then used to select one of these outputs.

Because the worst case delay through the chain of 74HC4017s will not allow all the possible outputs of the 74HC4051 to be re-clocked reliably to the same rising 10MHz clock edge as the 5Mhz and 1MHz signals, the output is initially re-clocked to the 1MHz signal used as input to the divider chain, and then to 10MHz. Separate 74AC74 D-flops (U18 and U19) are use to avoid cross modulation.

A dedicated output flip-flop package is used for each output frequency to avoid problems with simultaneous switching of two sets of logic in the same package.

The output stages

The outputs are driven by 74AC541 bus drivers. Four of the eight gates in each package are used. A 180 ohm resistor is used in series with the output of each gate, and the outputs are then commoned. The value of 180 ohms was chosen rather than 200 ohms because the 74AC541 output stages have non-zero output resistance, typically in the region of 25 ohms plus or minus 50%. This gives a close match to a 50 ohm load.

Construction Notes

If you haven't any previous experience of SMT soldering I suggest you look at the video tutorial entitled Surface Mount Soldering 101 which you will find at:

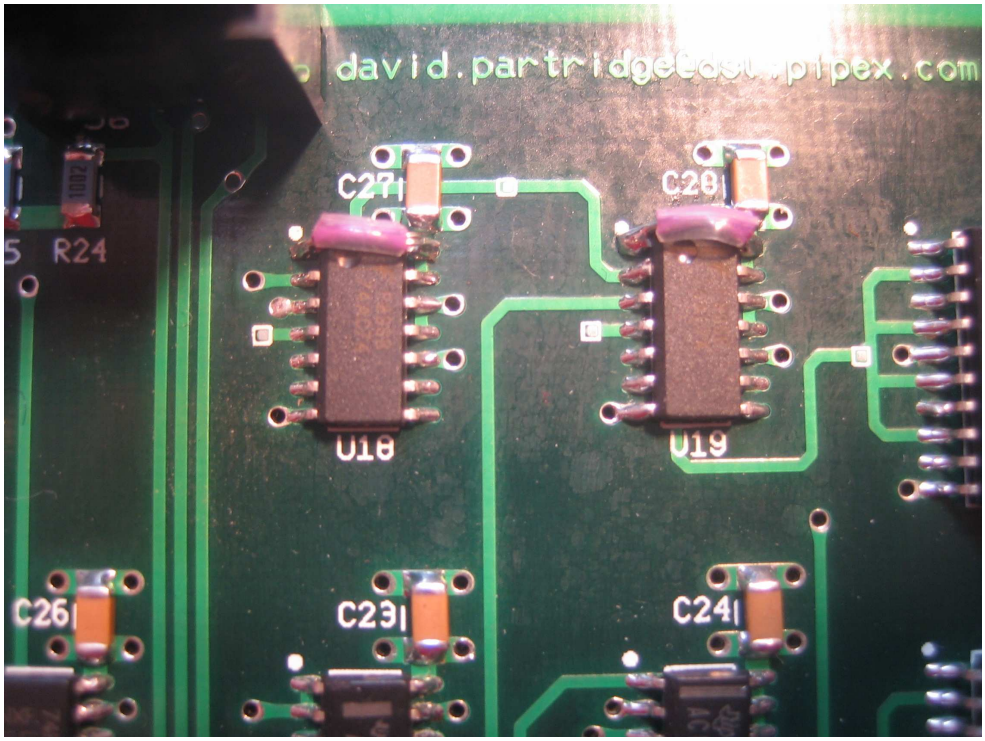
http://www.curiousinventor.com/guides/Surface_Mount_Soldering/101

Use a small tip soldering iron, and very fine solder, and install the smallest components first.

I suggest that you start with the BAV99 and MAX999 (D1 and U1). You may find it advantageous to use a very small dab of acrylic PCB lacquer to secure these before soldering them, as surface tension can easily pull these out of position. You can then install all the 1206 case size resistors and capacitors.

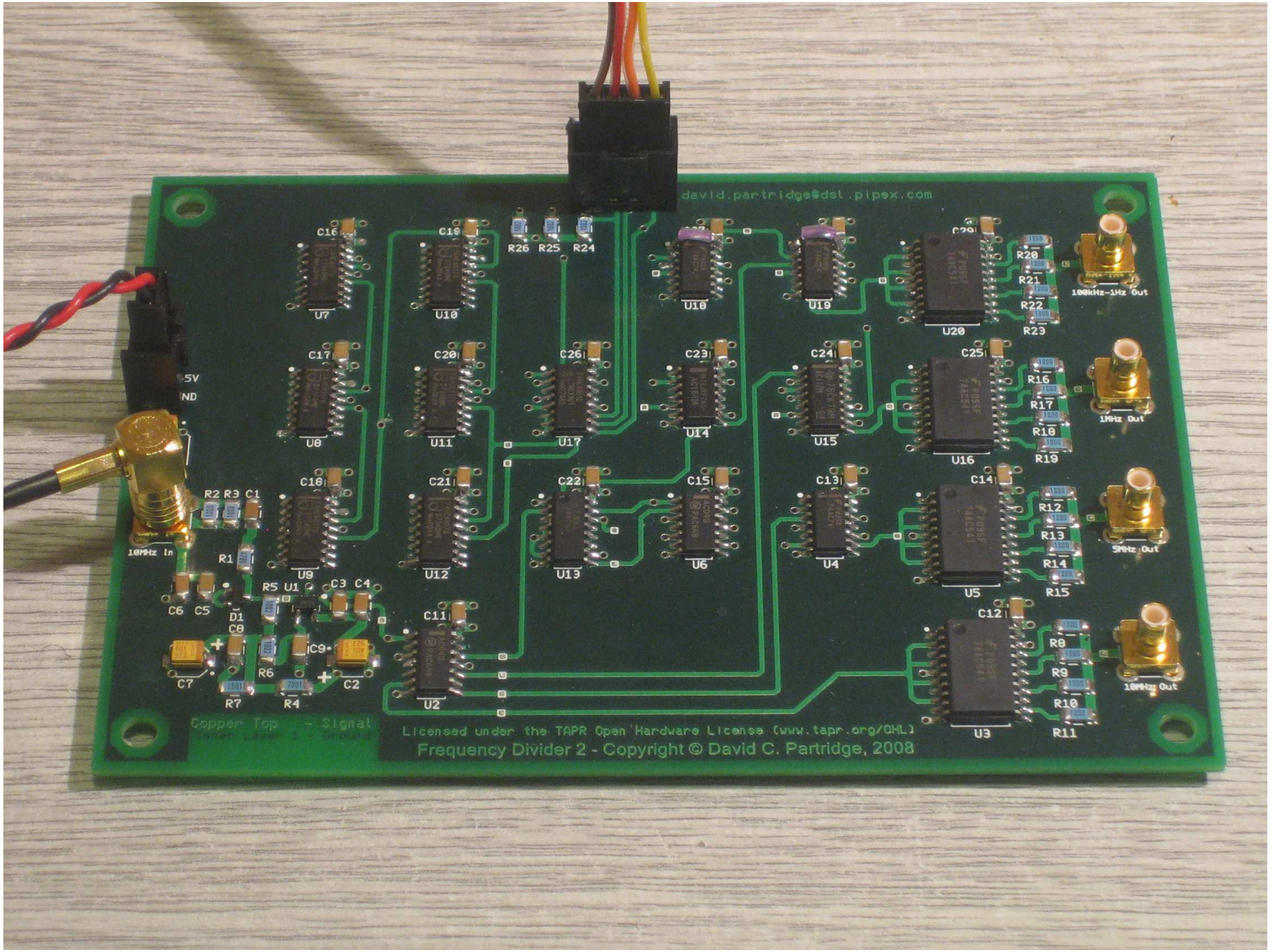
Once you've done all those, solder all the other ICs to the board, and finally add the electrolytic capacitors, headers, and SMA (or SMB) sockets.

There is a small problem with the first batch of PCBs manufactured in 2008 (without any revision number) which means that pin 1 of both U18 and U19 is not connected to Vcc as it should be. To fix this you can connect a short EC wire from pin 14 of these ICs to pin 1, across the top of the component. Or you can connect the EC wire from pin 1 to the via to the lower left of the decoupling capacitor.



The picture above shows these jumpers installed on the board.

The picture on the following page shows the completed divider.


david.partridge@dsl.pipex.com
10MHz In
100kHz-1Hz Out
1MHz Out
5MHz Out
10MHz Out
Copper Top - Signal
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